We are excited to announce a training program for the RISC-V-based SoC, Athos, its te st harness layer, Porthos, and integrating new IPs into Athos. The training will provide a good understanding of Athos SoC architecture, its software stack, and the hardware and software compilation flow with BCI verification and emulation flows (VeriForg e & ProtoForge). Participants will learn how to create new software tests, debug soft ware and hardware, and gain hands-on experience through labs using Verilator and Pall adium.

Athor is an innovative platform that serves as a chassis for building custom SOCs. The is training will cover the steps required to integrate an AI-accelerator IP into the Athor chassis, including hardware and software tasks. The training concludes with a top-down methodology for integrating new IPs and testing their integration.

Designed for both beginners and experienced users, this training program will be conducted for 7 to 8 hours, split into morning and afternoon sessions. At the end of the training, participants will thoroughly understand the methodology for integrating an IP into the Athos Chassis and the steps involved in hardware and software implementation. We look forward to your participation in this exciting training session.

Training Schedule

Chapter 1: Introduction to Athos \rightarrow (30 mins)

- Athos architecture
- Athos hardware
- Athos software
- Developing software on Athos

Chapter 2: Introduction to Porthos \rightarrow (30 mins)

- Early software development
- Requirements and challenges
- Emulation use models
- Difference between Virtual ICE vs. ICE
- Why Virtual ICE architecture
- Debug vs. Performance architectures
- Backdoor loading

Chapter 3: Introduction to Verification Flows \rightarrow (30 mins)

- Introduction to VeriForge flow
- Introduction to ProtoForge flow

Lab 1 - Introduction to Verification Flows \rightarrow (30 mins)

• Compile and run SW for Athos using VeriForge and ProtoForge

Lab 2 - Modifying Software to Run Verification Flow \rightarrow (60 mins)

- Modify an existing test case by making some changes (LOG_INFO()) and recompiling and running test
 - Learn how to use LOG_INFO
 - Learn how to use the software stack (DIF) for writing new tests
 - o Compile the new SW and run it on VeriForge
 - o Compile the new SW and run it on ProtoForge
 - A quick introduction to backdoor loading

Chapter 4: Debugging Athos using Porthos on Palladium \rightarrow (30 mins)

- Debug architecture
- Virtual peripheral components
- Debug interface

Lab 3 - Debugging using UART & Trace Log on Palladium \rightarrow (30 mins)

- Using the virtual UART
- Testing the virtual UART (input and output)
- Enabling trace log dumping
- Introduction to tracer and trace log

Chapter 5: Porthos Architecture for Performance → (15 mins)

- Details about DPI methods
- Details about UART DPI
- Profiling

Chapter 6: Extending Athos \rightarrow (15 mins)

- Overview of Athos as an extensible SOC chassis
- Explanation of the purpose and benefits of Athos

Chapter 7: Creation of Hardware Socket \rightarrow (30 mins)

- Explanation of the hardware tasks involved in integrating a custom IP into the Athos chassis
- Discussion of the hardware socket methodology
- A step-by-step description of each hardware task

Chapter 8: Creation of Software Socket \rightarrow (30 mins)

- Explanation of the software tasks involved in integrating a custom IP into the Athos chassis
- Discussion of the software socket methodology
- A step-by-step description of each software task

Chapter 9: Developing HW/SW sockets and integrating with Athos SoC

Chapter 10: Case Study: AI IPO8 Integration \rightarrow (30 mins)

- Overview of AI IPO8 and its role as an example for the training
- Description of the methodology used to integrate AI IPO8 into the Athos chassis
- Explanation of the hardware and software steps involved in the integration process
- Discussion of the results and outcomes of the AI IPO8 integration

Lab 4 - Integration of AI IPO8 \rightarrow (60 mins)

- Integrate a custom IP into the Athos chassis using the HW & SW socket methodol ogy.
- Run tests HW & SW tests using VeriForge.

Chapter 11: Conclusion \rightarrow (30 mins)

- Summary of the key points covered in the training
- Discussion of the next steps for participants after the training
- Opportunities for participants to ask any remaining questions or seek clarific ation on any topics covered in training.